0.5V VLSI Processor Circuit Technologies

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2. Circuit design at low voltage

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Trend of processor power

(Power consumption of processors published in ISSCC)

- Very High speed
- Large power
- High speed
- Low power

Crusoe
Published in Jan, 2000
Power < 6W
Power Crisis in VLSI processor

(ITRS: International Technology Roadmap for Semiconductors 1999)

174W Power in 2011 acceptable?
1. Background

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Power & Delay Dependence on $V_{DD} & V_{TH}$

\[ P = P_t f_{CLK} C_L V_{DD}^2 + \text{Leak power} \]

\[ t_{pd} = \frac{k C_L V_{DD}}{(V_{DD} - V_{TH})^\alpha} \]

$\alpha = 1.3$
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Controlling $V_{DD}$ and $V_{TH}$ for low power

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Multi-Threshold CMOS (MTCMOS)

Benefits
- Low leakage current in standby
  - Reduced by 3 or 4 orders of magnitude.

Issues
- Large leak cut-off transistor
- Difficult for ultra low voltage
- Need for special Flip Flop
Super Cut-Off CMOS (SCCMOS)

CMOS circuits
- low $V_{TH}$
- ultra thin $T_{OX}$

Leak cut-off switch
- low $V_{TH}$
- preferably thick $T_{OX}$

$V_{DD}$ can be decreased to 0.5V
$V_{TH}$ can be decreased to less than 0.2V
Delay characteristics

SCCMOS 0.2V $V_{TH}$ circuit with 0.2V $V_{TH}$ cut-off MOSFET

MTCMOS 0.2V $V_{TH}$ circuit with 0.6V $V_{TH}$ cut-off MOSFET

Conventional All 0.6V circuit No cut-off MOSFET

Standby current = 1pA
Controlling $V_{DD}$ and $V_{TH}$ for low power

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Dual-Threshold Voltage technique

Critical paths $\rightarrow$ Low-$V_{TH}$ MOS
$\rightarrow$ High leakage, High speed

Non-critical paths $\rightarrow$ High-$V_{TH}$ MOS
$\rightarrow$ Low leakage, Low speed
## Controlling $V_{DD}$ and $V_{TH}$ for low power

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Dual Supply Voltage scheme

Critical paths $\rightarrow$ High-$V_{DD}$ $\rightarrow$ High speed

Non-critical paths $\rightarrow$ Low-$V_{DD}$ $\rightarrow$ Low power

Needs high speed level converter.
Controlling $V_{DD}$ and $V_{TH}$ for low power

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Variable Supply Voltage scheme (VS)

$V_{DD}$: External voltage

DC-DC Converter

Controller

Speed Detector

$V_{DD,IN}$: Required frequency

$T_{cp}$: Delay time of critical path

$T_{CLOCK}$: Clock cycle

- $T_{cp} > T_{CLOCK}$ ↔ “+” ↔ $V_{DD,IN}$
- $T_{cp} = T_{CLOCK}$ ↔ No change
- $T_{cp} < T_{CLOCK}$ ↔ “-“ ↔ $V_{DD,IN}$
1. Background
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4. Low voltage SRAM memory cell
   
   Memory in processor requires high speed

5. Summary
Low voltage SRAM memory cells

Lowering $V_{DD}$ of SRAM cell is difficult.

- Long wire
- Large capacitance
  - Needs strong current supply.
- Leak
  - Data will be lost.
0.5-1V $V_{DD}$ SRAM

- $V_{DD}=0.5V$
- High-$V_{TH}=0.35V$
- Low-$V_{TH}=0.15V$

- Write-port and Read-port are divided in order to cut read error.
- Precharge level of Bit line is low because of leakage at low-$V_{TH}$ MOS.

Low precharge  →  Low speed
High-$V_{TH}=0.35V$  →  Low reliability
Summary

Low power technologies will be most important technologies for future VLSI processor.

- **Low voltage logic technologies**

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- **Low voltage SRAM memory cell**
Future VLSI processor

For portable
• Ultra low $V_{DD}$ (<0.5V)
• High frequency (>1GHz)
• Low power (<10W)

For High-end machine
• Low $V_{DD}$ (>0.5V)
• Very high frequency (>10GHz)
• Large power (>100W)

Now → time